What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising:

a plurality of planar memory arrays, each planar memory array comprising a plurality of resistive memory cells arranged in rows and columns, the memory cells of a column being commonly coupled to a sense line, each sense line of an array being commonly electrically coupled to an associated sense line of each of said other memory arrays, each of said memory cells having an associated read line; and

an access transistor for electrically connecting said commonly electrically coupled sense lines to a sense amplifier during a read operation.

2. A memory device as in claim 1, wherein said resistive memory cells are magnetic resistive memory cells.

3. The memory device of claim 1, wherein said plurality of planar memory arrays are arranged in a vertical stack.

4. The memory device of claim 1, wherein each said memory cell has an associated sense line and read line, wherein said associated read line and said sense line are orthogonal to each other.

5. The memory device of claim 4, wherein each said read line is used to select an associated memory cell for a read operation.

6. The memory device of claim 5, wherein each said read line is also used to write to an associated memory cell.

7. The memory device of claim 4, further comprising a control line connected to a gate of said access transistor for enabling said access transistor during a read operation of a memory cell coupled to one of said sense lines.

8. The memory device of claim 4, further comprising a row decoder for activating a read line of a selected memory cell, a column decoder for selecting said access transistor, and a planar memory array decoder for selecting a memory array.

9. The memory device of claim 4, wherein all of the memory cells in a column of each said planar array are commonly coupled to said access transistor.

10. A memory device comprising:

a stack of memory cell planes, each of said memory cell planes comprising:

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells arranged in a column being coupled to an associated column sense line;

an interconnect line for interconnecting one column sense line of each of said stacked planes; and

an access transistor for coupling said interconnect line to a sensing circuit.

11. A memory device as in claim 10, wherein said interconnect line interconnects the same column sense line in each of said stacked planes together.

12. A memory device as in claim 11, wherein said interconnect is substantially vertical and runs through each of said stacked memory cell planes.

13. A memory device as in claim 10, wherein said sensing circuit comprises a sense amplifier having a first input coupled to said access transistor and a second input coupled to receive a reference signal.

14. A memory device as in claim 10 further comprising:

a plurality of interconnect lines each for interconnecting an associated one of the column sense lines of each of said stacked memory cell planes; and

a plurality of access transistors each coupling a respective interconnect line to a sensing circuit.

15. A memory device as in claim 10 further comprising:

a plurality of interconnect lines each for interconnecting an associated one of the column sense lines of each of said stacked memory cell planes; and

a plurality of access transistors each coupling a respective interconnect line to a respective sensing circuit.

16. A memory device as in claim 14, wherein the associated one of the column sense lines from each of said stacked memory cell planes are arranged in a vertical column sense line stack.

17. A memory device comprising:

a plurality of memory slices, each memory slice comprising a plurality of MRAM memory cells arranged vertically and horizontally in a plane and

which are commonly electrically coupled to a respective sense line interconnect; and

a plurality of access transistors, each electrically coupled to a respective sense line interconnect of a memory slice, each access transistor operating during a read operation to couple a selected memory cell in a slice to a sense amplifier.

18. The memory device of claim 17, wherein each memory cell has an associated read line.

19. The memory device of claim 18, wherein during a read operation said read line is selected by a row decoder, said access transistor is selected by a column decoder.

20. A memory device comprising:

a plurality of access transistors each adapted to be electrically coupled with a sense amplifier;

a plurality of memory slices, each memory slice comprising a stacked plurality of columns of commonly electrically coupled memory cells, each column of commonly electrically coupled memory cells being electrically coupled to a respective sense line; and

a plurality of sense line interconnects, each said sense line interconnect being electrically coupled between a respective access transistor and the sense lines of a respective memory slice.

21. A memory device as in claim 20 further comprising:

a plurality of sensing circuits, each said sensing circuit coupling to said respective access transistor.

22. The memory device of claim 20, further comprising a plurality of read lines respectfully associated with said memory cells for selecting an associated memory cell for a read operation.

23. A method of fabricating a memory device, said method comprising:

forming an access transistor over a substrate, said access transistor having a first and a second active area and a gate;

forming a substantially vertical memory slice having a plurality of stacked columns of memory cells coupled to a common sense conductor; and

forming a conductive path between said sense conductor and one of said active areas of said access transistor.

24. The method of claim 23, further comprising forming a sense amplifier which can be electrically coupled to said access transistor.

25. A method of fabricating a memory device, said method comprising:

forming an access transistor on a substrate, said access transistor having a first and a second active area and a gate;

forming a plurality of stacked planar memory array layers, each having rows and column of magnetic resistive memory cells; and

forming a first conductive path between a plurality of memory cells within a column of each of said planar memory array layers and one of said active areas of said access transistor.

26. A memory device as in claim 25, wherein said resistive memory cells are magnetic resistive memory cells.

27. The method of claim 25, further comprising forming said planar memory array layers in a vertical stack over said substrate.

28. The method of claim 27, further comprising forming a second conductive path between other of said active area of said access transistor and a sense amplifier.

29. The method of claim 27, further comprising forming a sense amplifier which can be electrically coupled with the other of said active area of said respective access transistor.

30. The method of claim 27, wherein said first conductive path is formed in a substantially vertical plane above said substrate.

31. The method of claim 31, further comprising a sense amplifier which can be electrically coupled with the other of said active area of said respective access transistor.

32. A method of reading selected resistive memory cells arranged in vertically stacked columns, each column containing a plurality of memory cells, said method comprising:

enabling an access transistor to commonly couple one side of said plurality of memory cells to a sense amplifier;

activating a row line conductor on another side of a selected memory cell of said vertically stacked columns of cells; and

sensing a resistive value of said selected memory cell with said sense amplifier.

33. The method of claim 32, further comprising:

enabling said access transistor in response to the output of a column decoder, and activating said row line in response to an output of a row decoder and a plane decoder which selects a plane associated with one of said vertically stacked columns of memory cells.

34. A method of reading a resistive memory device comprising a plurality of stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns, said method comprising:

accessing a selected memory cell by activating a row line coupled to a first side of said selected memory cell and turning on an access transistor which couples a second side of a plurality of memory cells in the same column of each said layer, to a sense amplifier.

35. A method as in claim 34, wherein said resistive memory cells are MRAM memory cells.

36. A method as in claim 34 further comprising sensing a resistance value of a selected memory cell with said sense amplifier.

37. A method of reading a resistive memory device comprising a plurality of stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns, said method comprising:

decoding a selected memory cell address as a column select signal, a row select signal, and a layer select signal;

using said layer select signal to select one of said layers for a read operation;

using said row select signal to select a row of memory cells of said selected one layer; and

using said column select signal to select the same column of memory cells in each of said layers by turning on an access transistors coupled to said same columns.

38. A method as in claim 37, wherein said resistive memory cells are MRAM memory cells.

39. A method as in claim 38 further comprising sensing a resistance value of a selected memory cell with a sense amplifier coupled to said access transistor.

40. A computer system comprising:

a central processing unit; and

a memory device electrically coupled to said central processing unit, said memory device comprising:

a plurality of planar memory arrays, each planar memory array comprising a plurality of resistive memory cells arranged in rows and column, the memory cells of a column being commonly coupled to a sense line, each sense line of an array being commonly electrically coupled to an associated sense line of each of said other memory arrays, each of said memory cells having an associated read line; and

an access transistor for electrically connecting said commonly electrically coupled sense lines to a sense amplifier during a read operation.

41. A computer system as in claim 40, wherein said resistive memory cells are magnetic resistive memory cells.

42. The computer system of claim 40, wherein said plurality of planar memory arrays are arranged in a vertical stack.

43. The computer system of claim 40, wherein each said memory cell has an associated sense line and read line, wherein said associated read line and said sense line are orthogonal to each other.

44. The computer system of claim 43, wherein each said read line is used to select an associated memory cell for a read operation.

45. The computer system of claim 44, wherein each said read line is also used to write to an associated memory cell.

46. The computer system of claim 43, further comprising a control line connected to a gate of said access transistor for enabling said access transistor during a read operation of a memory cell coupled to one of said sense lines.

47. The computer system of claim 43, further comprising a row decoder for activating a read line of a selected memory cell, a column decoder for selecting said access transistor, and a planar memory array decoder for selecting a memory array.

48. The computer system of claim 43, wherein all of the memory cells in a column of each said planar array are commonly coupled to said access transistor.

49. A computer system comprising:

a central processing unit; and

a memory device electrically coupled to said central processing unit, said memory device comprising:

a stack of memory cell planes, each of said memory cell planes comprising:

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells arranged in a column being coupled to an associated column sense line;

an interconnect line for interconnecting one column sense line of each of said stacked planes; and

an access transistor for coupling said interconnect line to a sensing circuit.

50. A computer system as in claim 49, wherein said interconnect line interconnects the same column sense line in each of said stacked planes together.

51. A computer system as in claim 50, wherein said interconnect is substantially vertical and runs through each of said stacked memory cell planes.

52. A computer system as in claim 49, wherein said sensing circuit comprises a sense amplifier having a first input coupled to said access transistor and a second input coupled to receive a reference signal.

53. A computer system as in claim 49 further comprising:

a plurality of interconnect lines each for interconnecting an associated one of the column sense lines of each of said stacked memory cell planes; and

a plurality of access transistors each coupling a respective interconnect line to a sensing circuit.

54. A computer system as in claim 49 further comprising:

a plurality of interconnect lines each for interconnecting an associated one of the column sense lines of each of said stacked memory cell planes; and

a plurality of access transistors each coupling a respective interconnect line to a respective sensing circuit.

55. A computer system as in claim 53, wherein the associated one of the column sense lines from each of said stacked memory cell planes are arranged in a vertical column sense line stack.

56. A computer system comprising:

a central processing unit; and

a memory device electrically coupled to said central processing unit, said memory device comprising:

a plurality of memory slices, each memory slice comprising a plurality of MRAM memory cells arranged vertically and horizontally in a plane and which are commonly electrically coupled to a respective sense line interconnect; and

a plurality of access transistors, each electrically coupled to a respective sense line interconnect of a memory slice, each access transistor operating during a read operation to couple a selected memory cell in a slice to a sense amplifier.

57. The computer system of claim 56, wherein each memory cell has an associated read line.

58. The computer system of claim 57, wherein during a read operation said read line is selected by a row decoder, said access transistor is selected by a column decoder.

59. A computer system comprising:

a central processing unit; and

a memory device electrically coupled to said central processing unit, said computer system comprising:

a plurality of access transistors each adapted to be electrically coupled with a sense amplifier;

a plurality of memory slices, each memory slice comprising a stacked plurality of columns of commonly electrically coupled memory cells, each column of commonly electrically coupled memory cells being electrically coupled to a respective sense line; and

a plurality of sense line interconnects, each said sense line interconnect being electrically coupled between a respective access transistor and the sense lines of a respective memory slice.

60. A computer system as in claim 59 further comprising:

a plurality of sensing circuits, each said sensing circuit coupling to said respective access transistor.

61. The computer system of claim 59, further comprising a plurality of read lines respectfully associated with said memory cells for selecting an associated memory cell for a read operation.